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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MERED, HABTE	

ART UNIT	PAPER NUMBER
2662	

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/927,359	SCHMIDT, STEVEN G	
	Examiner	Art Unit	
	Habte Mered	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/19/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 1-14** are rejected under 35 U.S.C. 102(b) as being anticipated by Rodiger et al (US 4, 991, 084), hereinafter referred to as Rodiger.

3. Regarding **claim 1**, *Rodiger discloses an NxM Round Robin Order Arbitrating Switching Matrix System* where a multiple arbitration circuit capable of simultaneously arbitrating multiple paths from n source ports to n destination ports at the same instance in time is included. **(See Column 1, Lines 30-40 and 54-57 and elements 42 in Figure 1; It should be noted that the system disclosed by Rodiger is a NXM crosspoint-switched matrix adopted to couple N inputs from N processor to M outputs where each output is a Basic Storage Module (BSM). N can be equal to M as is the case with Figure 1 where the input N equals 4 and the output M also equals 4.)**

4. Regarding **claim 2**, *Rodiger discloses an NxM Round Robin Order Arbitrating Switching Matrix System* wherein n represents the maximum number of ports on the corsspoint switched bus. **(See Column 1, Lines 31-32 and 60- 62; Rodiger discloses that there can be N inputs from N processors where N is variable and can be any value but ideally it can be 32 or greater.)**

5. Regarding **claim 3**, *Rodiger discloses an NxM Round Robin Order Arbitrating Switching Matrix System* further comprising a multiple arbitration unit **(Figure 1, elements 41-42 and Figure 3A, elements 301c-332c)** connected to the crosspoint switched bus **(Figure 1, elements 51-54 and Figure 3B, elements 301d-332d). (See also Column 1, Lines 54-57; Column 2, Lines 25-43; and Column 4, Lines 67-68)**

6. Regarding **claim 4**, *Rodiger discloses an NxM Round Robin Order Arbitrating Switching Matrix System* further comprising a multiple arbitration unit wherein the multiple arbitration units includes a request decoder for decoding a requested destination port. **(See Figure 3A, elements 301 a- 332a; Column 4, Lines 59-63)**

7. Regarding **claim 5**, *Rodiger discloses an NxM Round Robin Order Arbitrating Switching Matrix System* wherein the multiple arbitration unit includes a prioritizer for determining a destination address for each piece of data entering the circuit and then prioritizing data for each requested destination based on preprogrammed priority ranking. **(See Column 4, Lines 39-45; Rodiger discloses that when contention exists for two or more requests for a given output then the prioritizer mechanism in the arbitration unit then determines the destination address using a preprogrammed priority ranking called "round robin order".)**

8. Regarding **claim 6**, *Rodiger discloses an NxM Round Robin Order Arbitrating Switching Matrix System* wherein the multiple arbitration unit includes a crosspoint select encoder for decoding the output of the prioritizer and for encoding a crosspoint select value for the crosspoint switched bus. **(Figure 1, elements 51-54 and Figure 3B, elements 301d-332d;See Column 1, Lines 54-57; Column 2, Lines 25-43; and**

Column 4, Lines 39-45 and 67-68; Essentially the select encoders are the select switches that handle the output of the arbitration unit that contains the prioritizer. Therefore, element 80 in the applicant's Figure 1 can be viewed as part of the crosspoint and is equivalent to elements 301d-332d as shown in Rodiger's Figure 3B)

9. Regarding **claim 7**, *Rodiger discloses an NxM Round Robin Order Arbitrating Switching Matrix System* wherein the multiple arbitration unit includes an acknowledge OR for gathering acknowledges from the source ports and logically arranging the acknowledges based on predetermined characteristics. **(See element 100 in Figure 2;Column 3, Lines 1-7 and 41-52; and Column 4, Lines 39-45;Rodiger discloses that the gathered acknowledges from the source ports are arranged logically in a predetermined characteristics known as "round robin order".)**

10. Regarding **claim 8**, Rodiger discloses a switch having n non-blocking paths. **(See Column 1, Lines 55-56)**

11. Regarding **claim 9**, Rodiger discloses a multiple arbitration circuit **(Figure 1, elements 41-42 and Figure 3A, elements 301c-332c)** capable of simultaneously arbitrating multiple paths from at least one source port to at least one destination port through a switch comprising:

a crosspoint switch **(Column 1, Lines 54-57)** and a multiple arbitration unit, where the multiple arbitration unit comprises a request decoder **(301 a-332 a in Figure 3 A; and Column 4, Lines 59-62)**, a prioritizer **(Column 4, Lines 39-45)**, a crosspoint select encoder **(Figure 1, elements 51-54 and Figure 3B, elements 301d-332d)** and an

acknowledge OR **(element 100 in Figure 2;Column 3, Lines 1-7 and 41-52; and Column 4, Lines 39-45)**, wherein if a source port is requesting a destination port that no other source port is requesting, then the requested destination port can be arbitrated simultaneously with requests by source ports for other destination ports. **(See Column 1, Lines 30-40 and 54-57 and Column 4, Lines 46-51)**

12. Regarding **claim 10**, *Rodiger discloses an NxM Round Robin Order Arbitrating Switching Matrix System,* wherein the switch is a 32-port switch, and 32 ports can arbitrate for 32 separate destinations in a single arbitration cycle of the circuit. **(See Figures 3 A and 3B with 32 input ports ranging from 301 to 332; Column 4, Lines 50-57)**

13. Regarding **claim 11**, *Rodiger discloses an NxM Round Robin Order Arbitrating Switching Matrix System* a storage area network comprising a director switch. **(See Column 1, Lines 54-57 and 60-62 and Column 4, Lines 51-59. Since Rodiger's output are storage modules or servers and can constitute a storage area network. Director Switch is a terminology only used in storage area networks and refers to large switches in data centers with the important distinction of having ports greater or equal to 32. Rodiger's switch meets this definition.)**

14. Regarding **claim 12**, Rodiger discloses a method for making a director switch comprising the steps of obtaining a circuit and implementing the circuit in the director switch for the purpose of arbitrating data paths there through. **(See Column 1, Lines 30-40 and 54-57 and Figures 1-3)**

15. Regarding **claim 14**, *Rodiger discloses a* method interconnecting processors **(elements 11-14 in Figure 1)** and/or peripherals **(elements 21-24 in Figure 1)** through a switch employing a multiple arbitration circuit having a crosspoint switched bus **(See Figure 1)**, where the method comprises the steps of simultaneously arbitrating multiple paths from n source ports associated with the processors or the peripherals to n destination ports associated with the processors or peripherals at the same instance in time, wherein n represents the maximum number of ports on the crosspoint switched bus through the multiple arbitration circuit; **(Column 1, Lines 30-40 and 54-67 and Column 2, Lines 1-57)**

connecting at least one of the n destination ports to at least one of the n source ports **(Column 4, Lines 46-55).**

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. **Claim 13** is rejected under 35 U.S.C. 103(a) as being unpatentable over Rodiger et al (US 4, 991, 084), hereinafter referred to as Rodiger, in view of Cooke et al (US Pub. No. 2002/0073380), hereinafter referred to as Cooke.

Rodiger teaches a method for making a circuit usable in a switch having multiple source ports and multiple destination ports such that when a source port is requesting a destination port that no other source port is requesting, then the destination port can be

arbitrated simultaneously with requests by other source ports for other destination ports. **(See Column 1, Lines 30-40 and 54-67 and Column 2, Lines 1-57)**

Rodiger, however, fails to expressly disclose that the multiple arbitration circuit can be implemented via a procedure comprising the steps of configuring a field programmable gate array.

Cooke discloses a methodology for constructing re-usable circuit components using field programmable gate array (FPGA) **(See Paragraphs 37 and 118)**. Cooke teaches how an arbitration unit based on round robin order can be implemented **(See Paragraph 576).**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to implement Rodiger's arbitration unit using FPGA technology. The motivation is to realize flexible performance and soft programmability as FPGA allows the circuit to be reconfigurable.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Habte Mered whose telephone number is 571 272 6046. The examiner can normally be reached on Monday to Friday 9:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on 571 272 3088. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HM
03-22-2005

KENNETH VANDERPUYE
PRIMARY EXAMINER